Exhibit A

United States Patent and Trademark Office's February 3, 2022, Non-Final Rejection of Application No. 17/461,597

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2849	

NOTIFICATION DATE	DELIVERY MODE
02/03/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipntlaw@ipntlaw.com

Office Action Summary	Application No. 17/461,597	Applicant(s) AKER et al.	
	Examiner Thomas J Hiltunen	Art Unit 2849	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 8/30/21.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-27 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 1-14,24 and 26 is/are allowed.

7) ☑ Claim(s) 15-23,25 and 27 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 8/30/21 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date ______.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date ______.

4) ☐ Other: ______.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claim(s) 15-17, 19-20, 22-25 and 27 is/are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Chen et al. (USPN 6,995,603).

With respect to claim 15, Chen et al. discloses, in Figs. 3b, 6a and 6b, a charge pump architecture (Fig. 3b or Fig. 6a. Fig. 6a is essentially the same circuit as Fig. 3b expect having a different clocking scheme as shown in Fig. 6b. Thus, to aid in

explanation the rejections will be discussed with respect to Fig. 3b unless otherwise noted) comprising:

an input terminal (Vin) and an output terminal (Vout);

a first stage (31in) receiving a first voltage at its input terminal (Vin at the cross coupled MOSFETs of 31in) and outputting first and second boost voltages at its first and second output terminals, respectively (voltages at the anodes of C1 and C2, respectively, provided to the transistors of 31int1), the first stage including a first couple of capacitors connected to the first and second output terminals (C1;C2);

a first intermediate stage (31int1) receiving the first and second boost voltages at its first and second input terminals (inputs, e.g., source terminal, of the main cross-coupled NMOS transistors of 31int1, i.e., the NMOS transistors not included in the inverter circuits of the stage), respectively, from the first stage (31in) and outputting third and fourth boost voltages at its first and second output terminals, respectively, (voltages at the anodes of C3 and C4 output to 31int2) the first intermediate stage including a second couple of capacitors connected to its first and second output terminals (C3; C4);

a second or last intermediate stage (31int2) receiving the third and fourth boost voltages at its first and second input terminals (input, e.g., source terminal, of each the main cross-coupled NMOS transistors of 31int2), respectively, from the first intermediate stage (output from 31int) and outputting fifth and sixth boost voltages at its first and second output terminals (voltages at the anodes of C5 and C6), respectively, the second intermediate stage including a third couple of capacitors connected to its first and second output terminals (C5 and C6); and

a final stage (31out) receiving the fifth and sixth boost voltages at its first and second input terminals (voltages at the gate/drain terminals of the PMOS transistors), respectively, from the second intermediate stage (from 31int2) and outputting an output voltage at an output terminal (Vpp; Vpp terminal), wherein the input terminal of the charge pump architecture corresponds to the input terminal of the first stage and the output terminal of the charge pump architecture corresponds to the output terminal of the final stage (the charge pump is connected as claimed),

wherein the first stage includes:

the input terminal (Vin) and the first and second output terminals (voltages on the anodes of C1 and C2); and

a first type of MOS transistors transferring a voltage from the input terminal to the first and second output terminals and being cross-coupled (cross-coupled NMOS transistors of 31in directly connected to Vin transferring Vin to the anodes of C1 and C2),

wherein each of the first and second intermediate stages includes:

the first and second input terminals and the first and second output terminals (input terminals, e.g., sources, of the main cross-coupled NMOS transistors and output terminals, e.g., drains, of the main-cross coupled NMOS transistors);

a second type of MOS transistors transferring the boost voltages from the first and second input terminals of the stage to the first and second output terminals of the stage (the main cross-coupled transistors generating outputs at the anodes of the capacitors according to the first and second input terminals);

a third type of MOS transistors connecting gates of the second type of MOS transistors of the stage to the first and second input terminals of the stage (NMOS transistors within the inverters connected to the gates of the main cross-coupled NMOS transistors); and

a fourth type of MOS transistors connecting the gates of the second type of MOS transistors of the stage to the first and second output terminals of the stage (PMOS transistors of the inverters connected to the gates of the main cross-coupled NMOS transistors) , and

wherein the final stage includes:

the first and second input terminals (inputs to the cross-coupled PMOS transistors) and the output terminal (VPP terminal); and

a fifth type of MOS transistors (PMOS transistors of 31out) transferring the fifth and sixth boost voltages from the first and second input terminals of the stage to the output terminal of the stage and being cross-coupled (31out is connected and operative as claimed).

With respect to claim 16, the charge pump architecture of claim 15, wherein the final stage includes fifth types of MOS transistors transferring the boost voltages outputted by the second or last intermediate stage to the output terminal and being cross coupled (31out is connected and operative with 31int2 as claimed).

With respect to claim 17, the charge pump architecture of claim 16, wherein the first stage includes:

the input terminal (Vin);

the first couple of capacitors (C1 and C2) respectively driven by a clock signal and an inverted clock signal (CLK1 and CLK2);

the first output terminal, connected to a first capacitor of the first couple and a second output terminal, connected to a second capacitor of the first couple (output terminals at the anodes of C1 and C2, respectively); and

the first type of MOS transistors including:

a first NMOS transistor of the first type inserted between the input terminal and the first output terminal and having a control terminal connected to the second output terminal (NMOS transistor between VIN and C1); and

a second NMOS transistor of the first type inserted between the input terminal and the second output terminal and having a control terminal connected to the first output terminal (NMOS transistor between VIN and C2).

With respect to claim 19, the charge pump architecture of claim 17, wherein each of the first and second intermediate stages comprises:

the first and second input terminals (inputs to the main cross-coupled NMOS transistors);

the couple of capacitors (C3-C6), being the second couple of capacitors of the first intermediate stage or the third couple of capacitors of the second intermediate stage, respectively driven by the inverted clock signal and the clock signal (the capacitors are connected and driven as claimed);

the first output terminal connected to a first capacitor of the couple (output connected to the ones C3 with C5 and C4 with C6 in each respective stage) the and the second output terminal connected to a second capacitor of the couple (other one of the

output terminals connected to the other ones of C3 with C5 and C4 with C6 in each respective stage); and

an intermediate switching block inserted between the first and second input terminals of the stage and the first and second output terminals of the stage (main cross coupled NMOS transistors connected to the anodes of C3-C6), and including:

a first switching transistors structure inserted between the first input terminal of the stage and the first output terminal of the stage (one of the main cross-coupled NMOS transistors of 31int1 and 31int2 with the transistors of the inverter connected to the gate of the above transistor); and

a second switching transistors structure inserted between the second input terminal of the stage and the second output terminal of the stage (other one of the main cross-coupled NMOS transistors of 31int1 and 31int2 with the transistors of the inverter connected to the gate of the above transistor), wherein the first switching transistors structure and the second switching transistors structures are also connected to one another at the first and second input terminals of the stage (the circuit is connected and operative as claimed).

With respect to claim 20, the charge pump architecture of claim 19, wherein the first switching transistors structure includes:

a first internal circuit node (e.g., gate terminal of the transistor directly connected C4 of 31int1; gate terminal of the transistor directly connected to C5 of 31int2);

a first switching NMOS transistor of the second type inserted between the first input terminal of the stage and first output terminal of the stage (e.g., NMOS transistor connected between C1 and C4; NMOS transistor connected between C4 and C5) and

having a control terminal connected to the first internal circuit node (gate connected as claimed);

a first additional switching NMOS transistor of the third type inserted between the first input terminal of the stage and the first internal circuit node and having a control terminal connected to the second input terminal of the stage (e.g., NMOS transistor that is directly connected to C1 of the inverter connected between C1 and C3; NMOS transistor that is directly connected to C4 of the inverter connected between C4 and C6); and

a second additional switching PMOS transistor of the fourth type inserted between the first internal circuit node and the second output terminal of the stage and having a control terminal connected to the second input terminal of the stage (e.g., PMOS transistor with the gate directly connected to C4; PMOS transistor with the gate directly connected to C5), and wherein

the second switching transistors structure includes:

a second internal circuit node (e.g., gate terminal of the transistor directly connected C3 of 31int1; gate terminal of the transistor directly connected to C6 of 31int2);

a first switching NMOS transistor of the second type inserted between the second input terminal of the stage and the second output terminal of the stage (e.g., NMOS transistor connected between C2 and C3; NMOS transistor connected between C3 and C6) and having a control terminal connected to the second internal circuit node (gate connected as claimed when the main cross-coupled transistor(s) is/are activated);

a first additional switching NMOS transistor of the third type inserted between the second input terminal of the stage and the second internal circuit node and having a control terminal connected to the first input terminal of the stage (e.g., NMOS transistor that is directly connected to C2 of the inverter connected between C2 and C4; NMOS transistor that is directly connected to C3 of the inverter connected between C3 and C5); and

a second additional switching PMOS transistor of the fourth type inserted between the second internal circuit node and the first output terminal of the stage (e.g., PMOS transistor with the gate directly connected to C3; PMOS transistor with the gate directly connected to C6) and having a control terminal connected to the first input terminal of the stage (gate connected as claimed when the main cross-coupled transistor(s) is/are activated).

With respect to claim 22, the charge pump architecture of claim 20, wherein the final stage comprises:

the first (input to the PMOS transistor having a drain directly connected to C5) and second input terminals of the stage (input to the PMOS transistor having a drain directly connected to C6);

a first PMOS transistor of the fifth type inserted between the first input terminal of the stage and the output terminal (drain terminal of the PMOS transistor directly connected to C5); and

a second PMOS transistor of the fifth type inserted between the second input terminal of the stage and the output terminal (terminal of the PMOS having a drain directly connected to C6), and wherein the first PMOS transistor has a control terminal

connected to the second input terminal of the stage and the second PMOS transistor has a control terminal connected to the first input terminal of the stage (the gates of the PMOS transistors are connected as claimed).

With respect to claim 23, the charge pump architecture of claim 16, wherein a plurality of additional intermediate stages are connected serially (the stages are serially connected).

With respect to claim 25, the charge pump architecture of claim 19, wherein the clock signal and the inverted clock signal driving each of the stages are shifted from one another by a delay period, inserted in the clock signal and inverted clock signal driving a stage to anticipate the shifted clock signals with respect to the clock signal and the inverted clock signal of a previous stage (PCLK1-PCLK6 of Fig. 6a are generated as claimed, see the delays as shown in Fig. 6b).

With respect to claim 27, a charge pump architecture comprising:

an input stage (31in) suitable for receiving an input voltage (Vin) and outputting first and second boost voltages respectively through a first couple of boosting nodes (voltages at the anodes of C1 and C2);

a first intermediate stage (31int1) suitable for receiving the first and second boost voltages and outputting third and fourth boost voltages respectively through a second couple of boosting nodes (voltage at the anodes of C3 and C4);

a second intermediate stage (31int2) suitable for receiving the third and fourth boost voltages and outputting fifth and sixth boost voltages respectively through a third couple of boosting nodes (voltage at the anodes of C5 and C6); and

an output stage respectively suitable for receiving the fifth and sixth boost voltages (31out) and outputting an output voltage through an output node (Vpp; Vpp node), wherein the input stage includes:

a first couple of capacitors respectively connected to the first couple of boosting nodes (C1; C2); and

first-type MOS transistors respectively suitable for transferring the input voltage to the first couple of boosting nodes (the main cross-coupled NMOS transistors of 31in),

wherein the first intermediate stage includes:

a second couple of capacitors respectively connected to the second couple of boosting nodes (C3; C4);

second-type MOS transistors respectively suitable for transferring the first and second boost voltages to the second couple of boosting nodes (main cross-couple NMOS transistors of 31int1);

third-type MOS transistors respectively suitable for connecting gates of the second-type MOS transistors thereof to the first couple of boosting nodes (NMOS transistors of the inverters of 31int); and

fourth-type MOS transistors respectively suitable for connecting the gates of the second-type MOS transistors thereof to the second couple of boosting nodes (PMOS transistors of the inverters of 31int),

wherein the second intermediate stage includes:

a third couple of capacitors respectively connected to the third couple of boosting nodes (C5;C6);

second-type MOS transistors respectively suitable for transferring the third and fourth boost voltages to the third couple of boosting nodes (main cross-coupled NMOS transistors of 31int2);

third-type MOS transistors respectively suitable for connecting gates of the second-type MOS transistors thereof to the second couple of boosting nodes (NMOS transistors of the inverters of 31int2); and

fourth-type MOS transistors respectively suitable for connecting the gates of the second-type MOS transistors thereof to the third couple of boosting nodes (PMOS transistors of 31int2), and

wherein the output stage includes fifth-type MOS transistors respectively suitable for transferring the fifth and sixth boost voltages to the output node (PMOS transistors of 31out).

Claim(s) 15-18 is/are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Yamahira (USPAPN 2008/0169864).

With respect to claim 15, Yamahira discloses, in Fig. 8, a charge pump architecture (Fig. 8) comprising:

an input terminal (110) and an output terminal (Vpump);

a first stage (852 with 855) receiving a first voltage at its input terminal (voltage on 110) and outputting first and second boost voltages at its first and second output terminals, respectively (voltage at 111; voltage at 114), the first stage including a first couple of capacitors connected to the first and second output terminals (each 910 of 852 and 855);

a first intermediate stage (853 with 856) receiving the first and second boost voltages at its first and second input terminals (inputs of 853 and 856), respectively, from the first stage and outputting third and fourth boost voltages at its first and second output terminals, respectively, (voltages on 112 and 115) the first intermediate stage including a second couple of capacitors connected to its first and second output terminals (each 910 of 853 and 856);

a second or last intermediate stage (854 with 857) receiving the third and fourth boost voltages at its first and second input terminals, respectively, from the first intermediate stage (voltages on 112; 115) and outputting fifth and sixth boost voltages at its first and second output terminals (voltages at 113 and 116), respectively, the second intermediate stage including a third couple of capacitors connected to its first and second output terminals (each 910 of 854 and 857); and

a final stage (858 and 859) receiving the fifth and sixth boost voltages at its first and second input terminals respectively, from the second intermediate stage (voltages on 113 and 116) and outputting an output voltage at an output terminal (Vpump; Vpump terminal), wherein the input terminal of the charge pump architecture corresponds to the input terminal of the first stage and the output terminal of the charge pump architecture corresponds to the output terminal of the final stage (the charge pump is connected as claimed),

wherein the first stage (825 with 855 includes:

the input terminal (110) and the first and second output terminals (voltages on 111 and 114); and

a first type of MOS transistors transferring a voltage from the input terminal to the first and second output terminals and being cross-coupled (each 860 cross coupled via 862),

wherein each of the first and second intermediate stages (853 with 856; 854 with 857) includes:

the first and second input terminals (terminals connected to 111 and 114;112 and 112) and the first and second output terminals (terminals connected to 112 and 115; 113 and 116);

a second type of MOS transistors transferring the boost voltages from the first and second input terminals of the stage to the first and second output terminals of the stage (each 860);

a third type of MOS transistors connecting gates of the second type of MOS transistors of the stage to the first and second input terminals of the stage (each 861); and

a fourth type of MOS transistors connecting the gates of the second type of MOS transistors of the stage to the first and second output terminals of the stage (each 860) , and

wherein the final stage (858 with 859) includes:

the first and second input terminals (terminals connected to 113 and 116) and the output terminal (Vpump terminal); and

a fifth type of MOS transistors (each 860) transferring the fifth and sixth boost voltages from the first and second input terminals of the stage to the output terminal of

the stage and being cross-coupled (each 860 of the final stage is connected and operative as claimed).

With respect to claim 16, the charge pump architecture of claim 15, wherein the final stage includes fifth types of MOS transistors transferring the boost voltages outputted by the second or last intermediate stage to the output terminal and being cross coupled (858 and 859 are connected to 854 and 857 as claimed).

With respect to claim 17, the charge pump architecture of claim 16, wherein the first stage (852 with 855) includes:

the input terminal (110 terminal);

the first couple of capacitors (each 910) respectively driven by a clock signal and an inverted clock signal (CLK1 and CLK2);

the first output terminal, connected to a first capacitor of the first couple and a second output terminal, connected to a second capacitor of the first couple (910 connected to 111 and 910 connected to 114); and

the first type of MOS transistors including:

a first NMOS transistor of the first type inserted between the input terminal and the first output terminal and having a control terminal connected to the second output terminal (NMOS transistor 860 of 852 gate connected to second output via 862); and

a second NMOS transistor of the first type inserted between the input terminal and the second output terminal and having a control terminal connected to the first output terminal (860 of 855 gate connected to first output via 860).

With respect to claim 18, the charge pump architecture of claim 17, wherein the first NMOS transistor and the second NMOS transistor are triple-well NMOS transistors

(the NMOS transistors are triple well see paragraph 0081) having bulk terminals connected to their source terminals (source S connected to the bulk at PW)

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 21 is/are rejected under 35 U.S.C. 103 as being unpatentable over Chen et al. (USPN 6,995,603) in view of Yamahira (USPAPN 2008/0169864).

With respect to claim 21, Chen et al. fails to disclose the types of transistors that the NMOS transistors are constructed from and fails to explicitly disclose bulk connections of the NMOS and PMOS transistors. Thus, Chen fails to disclose “wherein the first switching NMOS transistor, the first additional switching NMOS transistor of the first switching transistors structure as well as the first switching NMOS transistor and the first additional switching NMOS transistor of the second switching transistors structure are triple-well transistors having bulk terminals connected to the source terminals, and wherein the second additional switching PMOS transistor of the first switching

transistors structure as well as second additional switching PMOS transistor of the second switching transistors structure have bulk terminals connected to the source terminals."

Nevertheless it is old and well-known to construct NMOS transistors of a charge pump using triple-well NMOS technology as well as connecting the source and bulk terminals of PMOS transistors of the charge pump together as well as connecting the bulk and source terminals of the triple-well NMOS transistors, for the purpose of, among other things, making it possible to suppress a decrease in charge transfer efficiency of the charge pump.

This is further evidenced in Fig. 8 of Yamahira which discloses a charge pump comprising NMOS transistors (e.g., 860, 861, etc.) constructed using triple-well technology (see paragraph 0002) and PMOS transistors having a source connected to its bulk (e.g., see 862, etc. having the source and backgate/bulk connected). The triple-well and source to bulk connections allow for, among other things, suppressing the substrate biasing effect to suppress a decrease in charge transfer efficiency (see paragraph 0011 and paragraph 0094).

It would have been obvious to one of ordinary skill in the art before the effective filing date of the invention to construct the NMOS transistors of Chen from triple-well technology as wells connect the source to the bulk terminals of the transistors for the purpose of, among other things, suppressing the substrate biasing effect to suppress a decrease in charge transfer efficiency.

Allowable Subject Matter

Claims 1-14, 24 and 26 are allowed

With respect to claim 1, no cited art discloses the input terminal, output terminal, first stage, second stage, auxiliary stage connected and operative as recited in claim 1 and "wherein each of the first stage and second stage comprises:

the input terminal and the output terminal of the stage;

a first type of MOS transistors transferring the **voltage from the input terminal to the couple of internal boosting nodes and being cross-coupled**; and

a second type of MOS transistors with their gate biased by a third type of MOS transistors and a fourth type of MOS transistors;

the third type of MOS transistors connecting the gates of the second type of MOS transistors to the couple of <u>internal boosting nodes of the stage</u>; and

the fourth type of MOS transistors connecting the gates of the second type of MOS transistors to the couple <u>of internal boosting nodes of the next stage</u>."

There is no cited art that discloses the first through fourth type of MOS transistors being connected and operative such that the input terminal, internal boosting nodes, and output terminals are distinct terminals in each of the first and second stages and the third type MOS transistors and fourth type MOS transistors being operative to connect the gates of the second type MOS transistors to the internal boosting node of the stage and the internal boosting nodes of the next stage, respectively.

Claims 2-14, 24 and 26 are allowed for similar reasons as claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached 9:00AM-5:30PM EST M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Menatoallah Youssef can be reached on 571-270-3684. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/THOMAS J. HILTUNEN/
Primary Examiner, Art Unit 2849